
HD74HCT564/HD74HCT574

Octal D-type Flip-Flops (with 3-state outputs)

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Description



These devices are positive edge triggered flip-flops. The difference between HD74HCT564 and HD74HCT574 is only that the former has inverting outputs and the latter has non-inverting outputs.

Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q or \bar{Q} outputs on positive going transitions of the clock (CK) input. When a high logic level is applied to the output control (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (D to Q, \bar{Q}) = 15 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

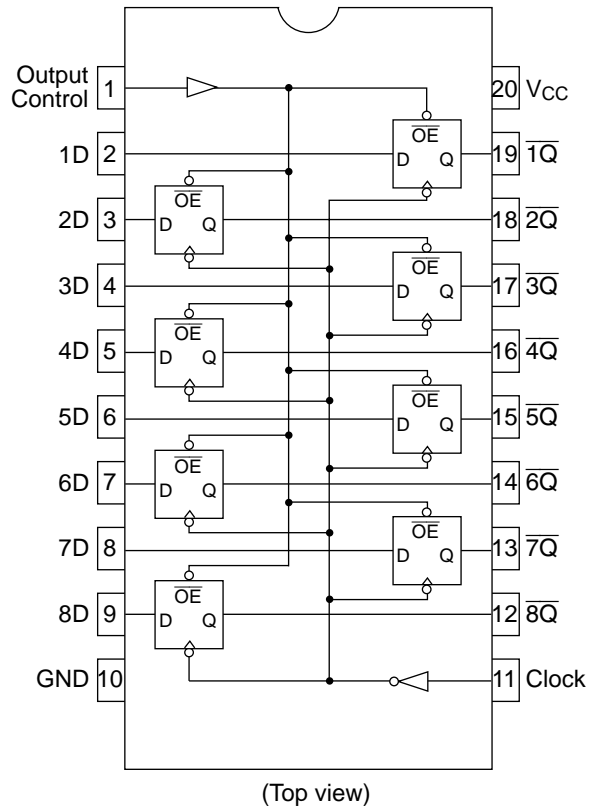
Function Table

Output Control	Clock	Data	Outputs	
			HD74HCT564	HD74HCT574
L		H	L	H
L		L	H	L
L	L	X	\bar{Q}_0	Q_0
H	X	X	Z	Z

HD74HCT564/HD74HCT574

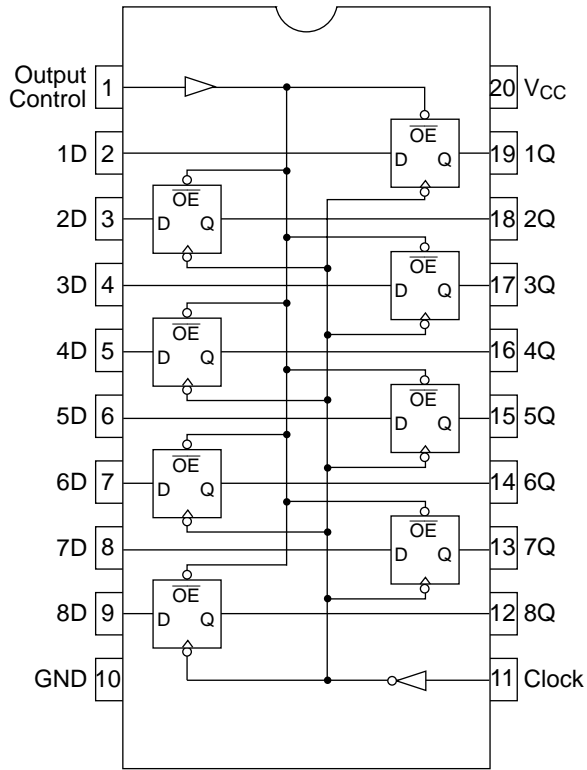
Pin Arrangement

HD74HCT564



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HD74HCT574

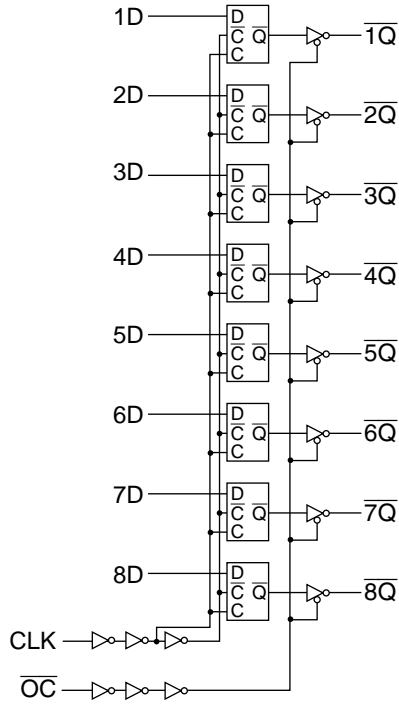


(Top view)

HD74HCT564/HD74HCT574

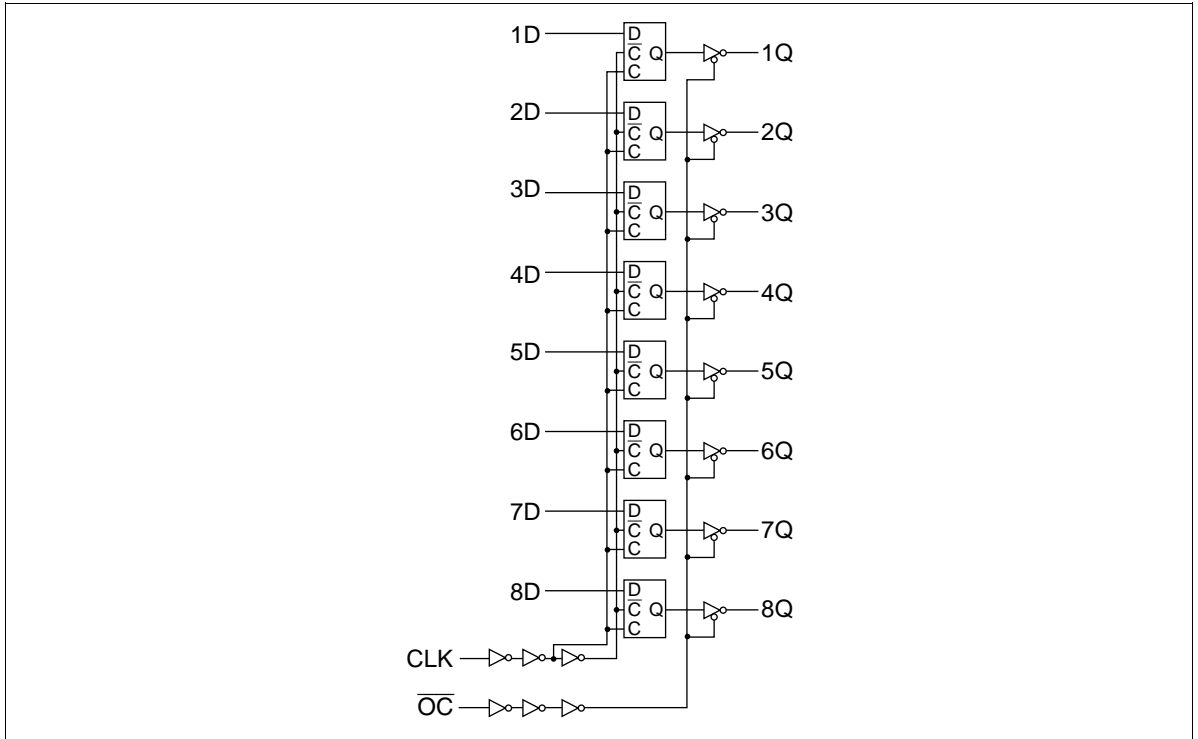
Block Diagram

HD74HCT564



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HD74HCT574



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC current drain per pin	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	$^{\circ}C$

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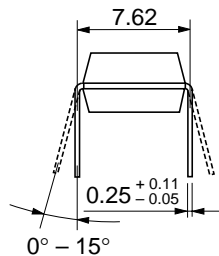
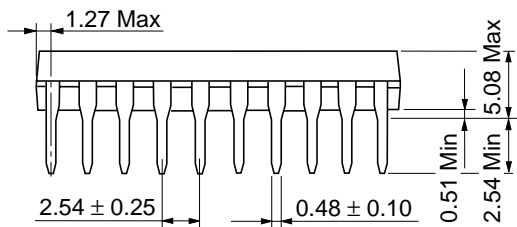
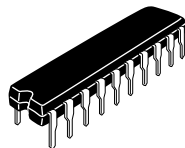
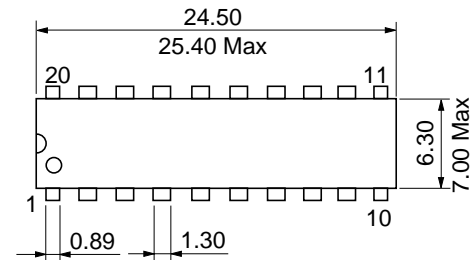
DC Characteristics

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
		Min	Typ	Max	Min		Max	V _{CC} (V)	
Input voltage	V _{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5	
	V _{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5	
Output voltage	V _{OH}	4.4	—	—	4.4	—	V	4.5	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA
		4.18	—	—	4.13	—		4.5	
	V _{OL}	—	—	0.1	—	0.1	V	4.5	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
		—	—	0.26	—	0.33		4.5	I _{OL} = 6 mA
Off-state output current	I _{OZ}	—	—	±0.5	—	±5.0	μA	5.5	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND
Input current	I _{in}	—	—	±0.1	—	±1.0	μA	5.5	Vin = V _{CC} or GND
Quiescent current	I _{CC}	—	—	4.0	—	40	μA	5.5	Vin = V _{CC} or GND, Iout = 0 μA

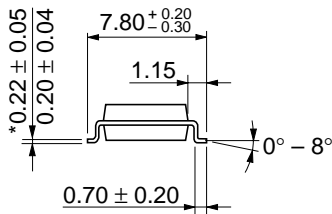
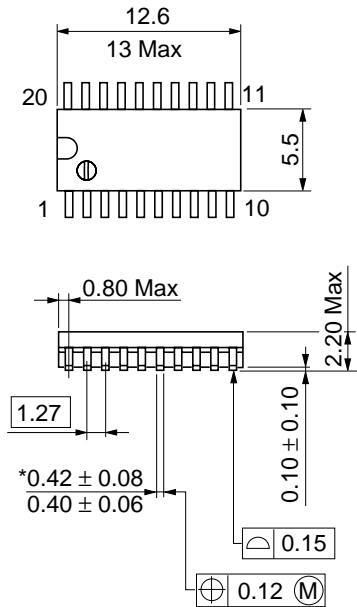
AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min		Max	V _{CC} (V)
Maximum clock frequency	f _{max}	—	—	30	—	24	ns	4.5
Propagation delay time	t _{PLH}	—	14	31	—	39	ns	4.5
	t _{PHL}	—	15	31	—	39		4.5
Output enable time	t _{ZL}	—	16	30	—	38	ns	4.5
	t _{ZH}	—	16	30	—	38		4.5
Output disable time	t _{LZ}	—	15	30	—	38	ns	4.5
	t _{HZ}	—	18	30	—	38		4.5
Setup time	t _{su}	12	3	—	25	—	ns	4.5
Hold time	t _h	5	-2	—	5	—	ns	4.5
Pulse width	t _w	16	7	—	20	—	ns	4.5
Output rise/fall time	t _{TLH}	—	4	12	—	15	ns	4.5
	t _{THL}	—	4	12	—	15		4.5
Input capacitance	C _{in}	—	5	10	—	10	pF	—

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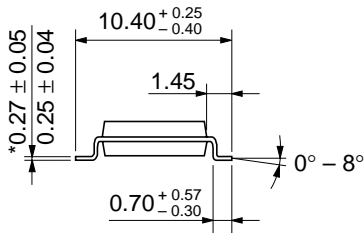
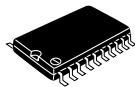
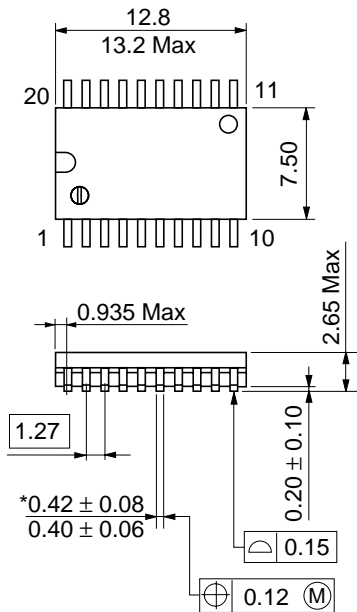


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



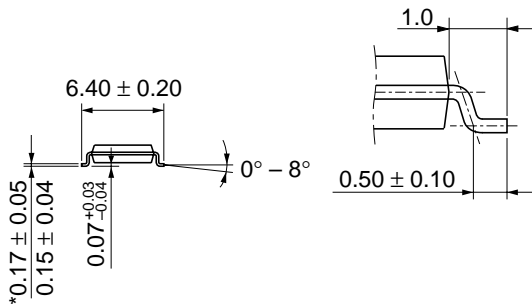
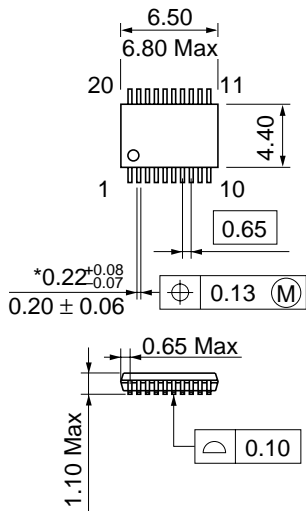
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
 Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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